REMARKS

Claims 1 to 16 have been examined. Claims 1, 2, 5, 8, 11, 12, and 14 have been amended. Claim 1 has been amended to incorporate features of claims 2, 4 and 5 as well as to correct informalities. Claim 2 has been amended to cancel the feature incorporated in claim 1. Claim 4 has been canceled as it has been incorporated into claim 1. Claims 5, 8, and 12 have been amended to correct informalities. Claim 11 has been amended as indicated below. Claim 14 has been amended to incorporate a feature of claim 5 and also to further clarify what is claimed as the invention. No new matter has been added.

Claims 1 to 3 and 5 to 16 are pending.

Claim Rejections - 35 USC §112

Claim 11 has been amended to obviate the antecedent problem. Support for the amendment is found, for example, at page 21, lines 4 to 12. No new matter has been added.

Claim Rejections - 35 USC §102

Claims 1, 4, 6, 7, 10, and 11 have been rejected as being anticipated by Fukutomi et al. The Examiner cites Fig. 22a-g as illustrating the present invention. However, Fukutomi et al. does not anticipate amended claim 1 as recited as follows:

> 1. (Amended) A semiconductor device comprising:
> a plurality of conductive paths electrically separated from one another by a trench;
> **a first conductive path of said plurality of conductive paths, having a die pad shape;**
> a semiconductor chip disposed on said first conductive path; **said first conductive path coupled to said semiconductor chip through a thermally conductive material;**
> a second conductive path disposed peripherally around said semiconductor chip, having a bonding pad shape;
> **a third conductive path having a shape of an external connecting pad and coupled to said second conductive path, said third conductive path being disposed underneath said semiconductor chip and coupled to said semiconductor chip through an insulating material;**
> connecting means for electrically connecting said semiconductor chip to said second conductive path;

insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conducive paths with a bottom surface of the paths exposed. (Emphasis added.)

That is, Fig. 22a-g of Fukutomi et al. do not show or describe (1) a first conductive path having a die pad shape, (2) the first conductive path coupled to said semiconductor chip through a thermally conductive material, (3) a third conductive path having a shape of an external connecting pad and coupled to the second conductive path, and the third conductive path being disposed underneath the chip and coupled to the chip through an insulating material, as claimed in claim 1.

Nowhere does Fukutomi et al. show or describe a conduction path shaped into a die pad. Furthermore, Fukutomi et al.'s semiconductor device 54 is bonded to the wiring patterns 63 by the die-bonding material 66. There is no description regarding whether any thermally conductive material is used between the device 65 and the wiring patterns 63. Indeed, the Fukutomi et al.'s teaching that the areas of the exposed wiring patterns 63 of Fig. 22g may be coated by a known solder resist ("...where the exposed wiring patterns are not protected by a corrosion-resistant metal such as nickel, areas other than the external connection terminal portions may be coated with a known solder resist or the like." column 23, line 67 to column 24, line 3) lends support that thermal conduction through the wiring patterns 63 was not considered and that the die-resist bonding material 66 was not designed with thermal conduction in mind.

Also, Fukutomi et al.'s wiring patterns 63 are formed by an electroplating process (column 23, lines 8 to 10). The wiring pattern 63 formed by an electroplating process would be extremely thin and would not work as a die pad.

Moreover, Fukutomi et al. does not show a structure as claimed in claim 1 where one of the conduction paths has a thermal conductive material placed thereon, and another conduction path has an insulating material placed thereon.

At least for these reasons, Fukutomi et al. does not anticipate the present invention of amended claim 1. Dependent claims 6, 7, 10, and 11 are also not anticipated at least for the same reasons as claim 1.

Claim 14 to 16 have been rejected as being anticipated by Kweon et al. However, Kweon et al. does not anticipate claim 14 as amended, which recites:

> 14. (Amended) A semiconductor device comprising:
> a plurality of conductive paths electrically separated from one another by a trench;
> **a semiconductor chip connected with at least one of said conductive paths through a thermal conductive material**; and
> insulating resin which covers said semiconductor chip, is embedded in the trench among said plurality of conductive paths and integrally supports the conducive paths, rear surface of which are at least partially exposed from the insulating resin,
> **wherein at least another one of said conductive paths is disposed at a periphery of said semiconductor chip and extends underneath the chip and coupled to the chip through an insulating material to form an external terminal.** (Emphasis added.)

Kweon et al. does not describe or show that at least another one of the conductive paths is disposed at a periphery of said semiconductor chip and extends underneath the chip and coupled to the chip through an insulating material to form an external terminal, as claimed in claim 14. In Fig. 15, Kweon et al. shows column leads 24 at the periphery of the chip 110, extending outwards from the package, but these column leads do not extend beneath the chip.

At least for the reasons above, claim 14 is not anticipated by Kweon et al. Dependent claims 15 and 16 are also not anticipated at least for the same reason as claim 14. Claim 14 is also not anticipated by Fukutomi et al. for the similar reasons as claim 1.

Claim Rejections - 35 USC §103

Claims 2, 3, 5 and 9 have been rejected as being unpatentable over Fukutomi et al. Fukutomi et al. does not teach or suggest the bolded features of claim 1 as recited above. Thus, these claims are non-obvious at least for the same reasons as claim 1.

Claims 8, 12, and 13 have been rejected as being unpatentable over Fukutomi et al. in view of Fjlstad and Kweon et al.

Claims 8, 12, and 13 would not have been obvious because the bolded features of amended claim 1 indicated above are neither taught nor suggested by Fukutomi et al. in view of Fjlstad and Kweon et al. The prior art references alone or in combination do not teach or suggest a structure as claimed in claim 1 where one of the conduction paths is disposed under the

semiconductor chip with a thermal conductive material placed therebetween, and another conduction path is disposed under the chip with an insulating material placed therebetween.

For the forgoing reasons, all pending claims are believed to be allowable over the cited art.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the specification:

Paragraph beginning at page 7, line 1 and ending at page 8, line 5 has been amended as follows:

[Description of the Related Art] Brief Description of the Drawings

[[Fig. 1]] Fig. 1 is a view for explaining a semiconductor device according to this invention.

[[Fig. 2]] Fig. 2 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 3]] Fig. 3 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 4]] Fig. 4 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 5]] Fig. 5 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 6]] Fig. 6 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 7]] Fig. 7 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 8]] Fig. 8 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 9]] Fig. 9 is a view for explaining a method of manufacturing a semiconductor device according to this invention.

[[Fig. 10]] Fig. 10 is a view for explaining a conventional mounting structure for a circuit device.

In the claims:

Claim 4 has been cancelled.

Claims 1, 2, 5, 8, 11, 12, and 14 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a plurality of conductive paths [which are] electrically separated from one another by a trench;

a first conductive path of said plurality of conductive paths, having a die pad shape;

a semiconductor chip [fixed] disposed on [a] said first conductive path [having a die pad shape of said plurality of conductive paths]; said first conductive path coupled to said semiconductor chip through a thermally conductive material;

a second conductive path disposed peripherally around said semiconductor chip, having a bonding pad shape;

a third conductive path having a shape of an external connecting pad and coupled to said second conductive path, said third conductive path being disposed underneath said semiconductor chip and coupled to said semiconductor chip through an insulating material;

connecting means for electrically connecting [a bonding electrode of] said semiconductor chip [and a] to said second conductive path [having a bonding pad shape; and];

insulating resin [which covers] covering said semiconductor chip, [is embedded] filling in the trench [among said plurality of conductive paths], and [supports and] integrally support[s]ing the semiconductor chip and the conducive paths with [their rear] a bottom surface of the paths exposed[,

wherein said second conductive path is formed outside said semiconductor chip and an external connecting pad is provided through a wiring extended from said second conductive path to the rear surface of said semiconductor chip].

2. (Amended) A semiconductor device according to claim 1 wherein said first conductive path has a smaller size than that that of the rear surface of said semiconductor chip,

[said second conductive path is formed outside said semiconductor chip, and

a third conductive path having a shape of an external connecting pad is provided through a wiring extended from said second conductive path to the rear surface of said semiconductor chip], said third conductive path has a larger size than that of said second conductive path.

5. (Amended) A semiconductor device according to claim 2, wherein [an] the insulating material is provided between said wiring extended to the rear surface of said semiconductor chip and said semiconductor chip or between said third conductive path and said semiconductor chip.

8. (Amended) A semiconductor device according to [of] claim 1, wherein the side of each of said conductive paths is curved to mate with said insulating resin.

11. (Amended) A semiconductor device according to claim 10, [wherein said] further comprising a conductive film selectively covering said conductive paths and having made of [the] material selected from the group consisting of nickel, silver and gold.

12. (Amended) A semiconductor device according to [of] claim 1, wherein said first conductive path is coupled with a conductive pattern formed on a mounting board through a thermally conductive material.

14. (Amended) A semiconductor device comprising:

a plurality of conductive paths [which are] electrically separated from one another by a trench;

a semiconductor chip connected with at least one of said conductive paths through a thermal conductive material; and

insulating resin which covers said semiconductor chip, is embedded in the trench among said plurality of conductive paths [and supports] and integrally supports the conducive paths, rear surface of which are at least partially exposed from the insulating resin,

wherein at least another one of said conductive paths is [connected with said semiconductor chip at external position of] disposed at a periphery of said semiconductor chip and extends [to the rear surface of] underneath the chip and coupled to the [said semiconductor] chip through an insulating material to [be] form an external terminal.